





Receiver Damage Threshold Per Lane	Pdag	dBm	+5.5	
------------------------------------	------	-----	------	--

### Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	oC	0		70
Power Supply Voltage	Vcc	V	3.2	3.3	3.4
Data rate		Gb/s		103.125	112

### Products Characteristics (tested under recommended operating conditions)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
<b>Voltage Supply Electrical Characteristics</b>						
Supply Current Tx Section / Rx Section		A	-	-	3	1
Power Supply Noise	Vrip				2%	DC-1MHz
					3%	1-10MHz
Dissipation Class2	Pw	W			9	
Low Power Dissipation	Plow	W			2	
Inrush Current n 2	I-inrush	mA/usec			50	
Turn-off Current <sup>Class2</sup>	I-turnoff	mA/usec	-50			
<b>Different Signal Electrical Characteristics</b>						
Single Ended Data Input Swing		mV	55 -		525	
Single Ended Data Output Swing		mV	180 -		385	
Differential Signal Resistance	Output	Ω	80		120	
Differential Signal Resistance	Input	Ω	80		120	
<b>3.3V LVC MOS Electrical Characteristics</b>						
Input High Voltage	3.3VIH	V	2.0		Vcc+0.3	
Input Low Voltage	3.3VIL	V	-0.3 -		0.8	
Input Leakage Current	3.3IIN	uA	-10		+ 10	
Output High Voltage (I <sub>OH</sub> =100uA)	3.3VOH	V	Vcc-0.2 -		-	
Output Low Voltage	3.3VOL	V			0.2	

**NETS**

ООО "Группа Компаний "Сети"  
 Проектирование сетей, поставка оборудования,  
 оптимизация и поддержка IT-инфраструктуры.  
<https://NewNets.ru>

(I <sub>OI</sub> = 100uA)						
Minimum Pulse Width of Control Pin Signal	T_CNTL	us	100			
<b>1.2V LVC MOS Electrical Characteristics</b>						
Input High Voltage	1.2VIH	V	0.84		1.5	
Input Low Voltage	1.2VIL	V	-0.3		0.36	

Input Leakage Current	1.2IIN	uA	-100		+ 100	
Output High Voltage	1.2VOH	V	1.0		1.5	
Output Low Voltage	1.2VOL	V	-0.3		0.2	
Output High Current	1.2IOH	mA			-4	
Output Low Current	1.2IOL	mA	+4			
Input Capacitance	Ci	pF			10	
<b>Optical Transmitter Characteristics</b>						
Signaling Rate for Each Lane (100GbE)		Gbps	-	25.78125+/-		
Signaling Rate for Each Lane (OTU4)				100ppm		
Four Lane Wavelength Range	$\lambda_1$	nm	1294.53	1295.56	1296.59	
	$\lambda_2$		1299.02	1300.05	1301.09	
	$\lambda_3$		1303.54	1304.58	1305.63	
	$\lambda_4$		1308.09	1309.14	1310.19	
Side Mode Suppression Ratio	SMSR	dB	30		-	
Total Average Launch Power (100GbE)	Pt	dBm	-		10.5	
Total Average Launch Power(OTU4)					8.9	
Average Launch Power for Each Lane(100GbE)	Pa	dBm	-4.3		+4.5	2
Average Launch Power for Each Lane(OTU4)					-2.5	+2.9
Optical Modulation Amplitude for Each Lane	OMA	dBm	-1.3		4.5	3
Transmitter and Dispersion Penalty for Each Lanes(100GbE)		TDP			2.2	
Transmitter and Dispersion Penalty for Each Lanes(OTU4)		TDP			1.5	

Average Launch Power of Off Transmitter for Each Lanes	Poff	dBm	-		-30	
Extinction Ratio (100GbE)	EX	dB	4			
Extinction Ratio (OTU4)			7			
Maximum channel power difference		dB			5	
RIN20OMA		dB/Hz			-130	
Optical Return Loss Tolerance		dB			20	
Transmitter Reflectance		dB			-12	4
Eye Diagram	Compliant with IEEE 802.3ba-2010/G.959.1)					
<b>Optical Receiver Characteristics</b>						
Receive Rate for Each Lane(100GbE)		Gbps		25.78125+/-		
Receive Rate for EachLane(OTU4)				27.95249+/-		
Four Lane Wavelength Range	$\lambda_1$	nm	1294.53	1295.56	1296.59	
	$\lambda_2$		1299.02	1300.05	1301.09	
	$\lambda_3$		1303.54	1304.58	1305.63	
	$\lambda_4$		1308.09	1309.14	1310.19	
Overload Input Optical Power	Pmax	dBm	4.5			5
Total Input Optical Power(OTU4)	Pt	dBm			8.9	
Average Receive Power for Each Lane(100GbE)	Pin	dBm	-10.6		4.5	6&7
Average Receive Power for Each Lane(OTU4)			-8.8		2.9	
Receive Power In OMA for Each Lane	PinOMA	dBm	-		4.5	
Difference in Receive Power between Any Two		dBm	-		5.5	
Receiver Sensitivity in OMA for Each	Pmin	dBm			-8.6	8





30	PRG_CNTL1	Programmable Control 1 MSADefault: TRXIC_RST n , TX&RX ICs reset, "0 " :reset; "1"	I	3.3V LVCMOS	per CFP MSA Management Interface Specification		Pull-Up Note1
31	PRG_CNTL2	Programmable Control 2 MSADefault : Hardware Interlock LSB	I	3.3V LVCMOS			Pull-Up Note1
32	PRG_CNTL3	Programmable Control 3 MSA Default:Hardware Interlock MSB	I	3.3V LVCMOS			Pull-Up Note1
36	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up Note1
37	MOD_LOPW R	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up Note1
39	MOD_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2

## Hardware Alarm Pins

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
33	prg_alm1	Programmable Alarm 1 MSADefault:HIPWR_ON	O	3.3V LVCMOS	Active High per MDIO document		
34	PRG ALRM 2	Programmable Alarm 2MSA default:MOD_READY , Ready State has been reached	O	3.3V LVCMOS			
35	PRG ALRM3	Programmable Alarm 3 MSA Default: MOD FAULT	O	3.3V LVCMOS			
38	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull-Down Note1
40	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note1: Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP module

Note2: PuH-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP module

## Management Interface Pins(MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. The CFP MDIO pins are listed in the following table: Management Interface Pins \_\_\_\_\_

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
41	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
47	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
48	MDC	MDIO Clock	I	1.2V LVCMOS			
46	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
45	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
44	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			
43	PRTADR3	MDIO Physical Port address bit3	I	1.2V LVCMOS			
42	PRTADR4	MDIO Physical Port address bit4	I	1.2V LVCMOS			

## Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP hardware Signal Pins are listed in the following table.

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_a ssert		1	ms	Application Specific May depend on current state Condition when signal is applied .See
TX Disable Assert Time	T_off		100	us	

## High Speed Electrical Characteristics

Reference Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Q	
Frequency			161.1328125/644.53125		MHz	1/64 or 1/16 of electrical lane rate
Frequency Stability	$\Delta f$	-100		100	ppm	For Ethernet applications
		-20		20		For Telecom applications





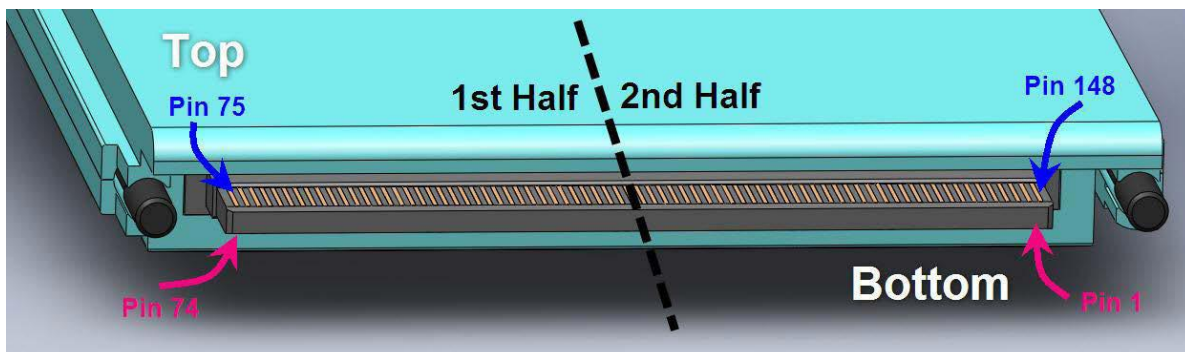
Output Differential Voltage	VDIFF	400		1200	mV	Peak to Peak Differential
RMS jitter1-2	0			10	ps	Random Jitter Over frequency band of 10KHz<f<10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	tr/f	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

Note1: The term "40GBASE\_FR" is the 40GbE serial optical interface in the task force phase at IEEE-SA at the time of this publication. Also, 1/16 of optical lane clock is recommended for TX\_MCLK and RX\_MCLK

Note2: Multi-protocol modules are recommended to adopt the clock rate rate used in Telecom applications

Optional Transmitter and Receiver Monitor Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Q	
Frequency					MHz	1/8 of Network lane rate
Output Differential Voltage	VDIFF	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	



Pad Layout of the CFP module

CFP Optical Interface lanes and Assignment

shows the orientation of the multimode fiber facets of the optical connector.

Mechanical Dimensions

